International Journal of Business and Management Invention
ISSN (Online): 2319 – 8028, ISSN (Print): 2319 – 801X
www.ijbmi.org || Volume 3 || Issue 4 || April 2014 || PP.14-27

Cost of Test Case Study for Multi-site Testing in Semiconductor Industry with Firm Theory

[1,] Voon C. Khoo M.Sc, MBA
[1,] *(School of Management, Asia e University, Malaysia)*

ABSTRACT: *This study investigated cost of test for the multi-site testing method in the semiconductor industry by using firm model theory. A cost of test model was developed based on firm average cost theory by integrating the technology aspect. This research aims to determine the effectiveness of multi-site testing method to reduce testing cost. The findings could provide the semiconductor industry with important guidelines for cost control to maintain profit margin in response to the depreciation of the average selling price in the past 20 years.*

KEYWORDS - *cost of test, testing economic model, multi-sites testing*

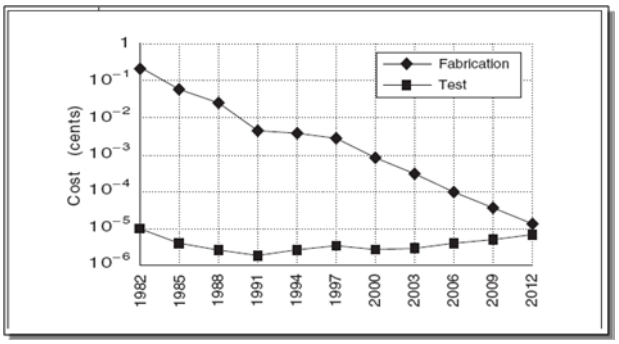
I. INTRODUCTION

Companies continuously reduce the selling price of electronic devices, including personal computers and cell phones, as a marketing strategy to maintain their position in the market and to stay competitive. For example, the Macintosh computer with a speed of 8 MHz was launched by Apple Inc. in 1984 and was sold at a price from US$1,995 to US$2,495 (http://en.wikipedia.org/wiki/Macintosh; cited: 11 April 2012). The latest generation of the Macintosh family, the iMac, is approximately a thousand times faster than the original Macintosh, and its speed ranges from 2.5 GHz to 3.1 GHz. This device is sold at a price that ranges from only $1,199 USD to $1,699 USD (http://store.apple.com/us/browse/home/shop_mac/family/imac/select; cited: 11 April 2012).

The latest Macintosh computers are 1000 times faster than previous models and have more advanced features. However, the price of these improved devices has decreased by approximately 47%. This situation shows that products with high-performance semiconductor chips are not sold at the same prices as 20 years ago.

Over the past 50 years, companies have been reducing fabrication cost by 25% to 30% (Goodall, 2002). Figure 1 shows that fabrication cost was predicted to decrease from US$0.1 per transistor in 1982 to US$0.0001 per transistor in 2012. However, testing costs have increased. In 2012, testing cost equaled fabrication cost (Bao, 2003).

Today, fabrication cost is no longer the deciding factor for the profit margin in manufacturing semiconductor chips. Therefore, semiconductor manufacturers must continuously improve their testing technology to reduce fabrication cost and the subsequent increase in testing cost. Accordingly, these manufacturers can stay competitive in the market if such improvement is persistently implemented. Failing to reduce testing cost will negatively affect the overall manufacturing cost of semiconductor chips in the future.



Source: Bao G. (2003)
Fig. 1 Gradual convergence between testing and fabrication costs for a transistor.

The design of new semiconductor chips must provide the flexibility and speed required by the increasing demand for high-complexity consumer electronic products. This trend shows that the functionality built into a single semiconductor chip today is substantially better than the functionality 20 years ago. However, testing costs in today's semiconductor industries can achieve a substantial percentage of the total manufacturing cost, thus affecting the profit margin.

Several approaches of reducing testing costs have been introduced. One of these approaches is multi-site testing, the effectiveness of which was determined by performing a case study. To achieve the research goal, a multi-site testing cost model was developed based on the economic theory of firm average cost by integrating important elements, including technology and multi-site efficiency, into the model. This study gauged the capabilities of the multi-site testing method to reduce testing costs by using the developed model.

The case studies were conducted on pick-and-place test equipment. Five multi-site configurations were set on the test equipment setup for comparison. Testing time, indexing time, and testing yield were collected to establish the testing cost. The hypothesis, which was designed to analyze the performance of the test equipment setup, is multi-site versus testing cost. The hypothesis was analyzed by using one-way ANOVA and post-hoc test.

This research identified that increasing the number of test sites cannot guarantee that testing cost will be reduced while maintaining profit margin because the testing time increases as the number of test sites increases. Accordingly, this research proposed that future work must use the multi-site testing approach together with other testing methods, including concurrent testing, which can reduce testing time.

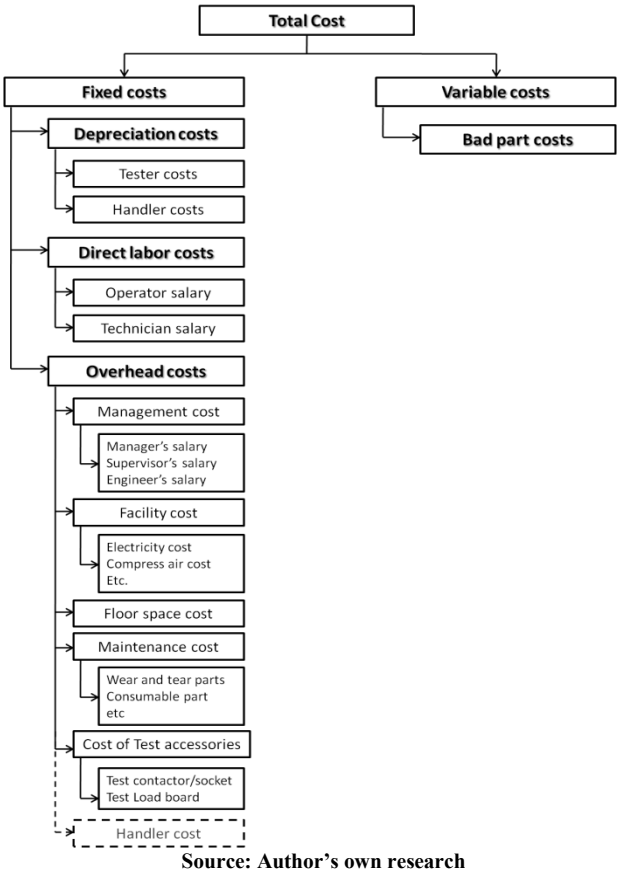
II. COST MODEL DEVELOPMENT

The cost of test model in this research was developed based on average cost theory, as shown in Equation 1. Average cost theory involves two elements, namely, total cost and production output.

$$\text{Average Total Cost (ATC)} = \frac{\text{Total Cost (TC)}}{\text{Output (Q)}} \quad (1)$$

A. Total Cost

According to average total cost theory, total cost includes fixed and variable costs. Figure 2 shows the variables, which affect the total cost, for the multi-site testing aspect.



Source: Author's own research

Fig. 2 Multi-site testing variables for total cost.

i. Fixed Cost

Fixed cost involves the cost of equipment depreciation (Dep), which includes tester and test handler costs. Equation 2 was developed to calculate equipment depreciation cost with a span of over five years from the purchase value to zero cost.

$$\text{Dep} = \left(\frac{\text{Tester Cost} + \text{Handler Cost}}{5} \right) \div 12. \quad (2)$$

The second variable that affects fixed cost is the direct labor cost (DL). DL cost is the monthly salary of employees, including operators and technicians, who directly contribute to the production output. DL cost is expressed as follows:

$$\text{Direct Labor Cost per month} = \left(\text{Operator salary per month} \times 3 \right) + \left(\text{Technician salary per month} \times 1.5 \right) \quad (3)$$

For the operator variable, each test equipment setup requires one operator. Thus, three operators are required each day to cover three production shifts, or one operator per shift. To standardize the equation for ease of understanding, three shifts are used in this study.

For the technician variable, one technician can support two test equipment setups. Therefore, only half the cost is required per test equipment setup. Only 1.5 technicians are involved in this study to cover three production shifts.

The wages of operators and technicians are based on a report published by JobStreet.com (cited: 11 April 2012). In this paper, the average wage is used as a reference for the aforementioned positions.

The overhead (OH) cost is the cost incurred during production and the costs of equipment depreciation and DL. OH cost includes the following elements:

- Management cost includes the monthly wages of manager, supervisor, and engineer. These wages are considered indirect labor costs. Data on wages are based on a JobStreet.com report (cited: 11 April 2012). Management cost is calculated by using the following formula:

$$\text{Management cost} = \text{Manager's Salary} + \text{Supervisor's Salary} + \text{Engineer's Salary} \quad (4)$$

- Facility cost is the monthly utility cost of electricity, compressed air, and so on.
- Floor-space (FPS) cost is the cost of the area occupied by the test equipment setup. The FPS cost is calculated as follows:

$$\text{FPS} = \left(\frac{\text{(Selling Price)}}{3000} \right) X \text{ Test Equipment floor space area (Sq-Ft)} \quad (5)$$

In this study, calculating the FPS cost is based on the 2011 report of the Valuation and Property Services Department of the Malaysian government. The 2011 "Detached House Pricing" is adopted as a reference for calculating price per square feet. The costs of test equipment setup FPS are then calculated by multiplying the required *X* number of area sq. ft. by the per sq. ft. pricing, as shown in Equation 5.

- Maintenance cost is the monthly expense of maintaining the test equipment. This expenditure includes wear-and-tear and consumable costs. This study estimates maintenance cost at 5% of the test equipment cost per year.

- Cost-of-test accessories include the test contactor and load board, which are described as follows:
  - Load board/probe card is the electronic printed circuit board used for interfacing between the tester and test handler.
  - Test contact socket is the mechanism used to connect the semiconductor device to the load board.

ii. Variable Cost

Variable cost is another factor identified as part of the total cost calculation that affects the test yield. From the research point of view, the variable cost is categorized as a changeable cost because it is not fixed, and it changes when the testing yield is modified.

Based on the test cost model developed by Rivoire (2003), the variable cost that must be included in the calculation is the bad-part cost. Bad-part cost is imperative in this research, particularly when dealing with multi-site configurations, because the developed model is validated by using this configuration. Changes may affect the consistency of the testing yield when the former is implemented during testing. The influence of such changes depends on the efficiency of multi-site repeatability.

To include the bad-part cost into the total cost equation, an equation has to be derived to calculate the former. The first step in deriving the bad-part cost equation is to imply the appropriate equation that can calculate the quantity of bad parts. Equation 6 is derived for this purpose.

$$\text{Number of bad part} = \text{Total Input X } \left[100\% - (\text{Testing Yield})\right] \quad (6)$$

Equation 6 denotes that the total incoming chip quantity is multiplied by the bad-part yield, which can be obtained by deducting the testing yield from 100%. The testing yield is the tested good part percentage that can be obtained from Equation 7.

$$\text{Testing yield \%} = \left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \text{ X } 100 \right) \quad (7)$$

Finally, to calculate the cost of the tested bad parts, the average selling price (ASP) of a particular type of semiconductor chip is multiplied by the number of bad parts obtained from Equation 6. Therefore, Equation 8 is derived to determine the total cost of tested parts.

$$C_{Pkg} = \text{ASP} \left[\text{Total Input X} \left(\text{ Bad part \% } \right) \right] \quad (8)$$

where
- C_{PKg} is the cost of bad parts;
- ASP is the average selling price;
- Total input is the total input of semiconductor chips; and
- Bad part % is the tested bad chips obtained by deducting the testing yield from 100%.

All costs are thoroughly discussed to facilitate the computation for total cost. The total cost is integrated, as shown in Equation 9, by combining all equations.

$$\text{Total Cost} = \text{Dep} + \text{DL} + \text{OH} + C_{Pkg.} \quad (9)$$

Production output is another element incorporated in average cost theory for the developed model. A detailed discussion of this element is provided in the subsection that follows.

B. Production Output

Production output consists of three fundamentals, namely, testing output (throughput), testing yield, and equipment utilization percentage. Detailed explanations of these fundamentals are presented below.

$$UPH_{good} = \frac{3600 \text{ X N}}{((1\text{-MSE})(N\text{-}1)(t_1+i_1) + (t_1+i_1))} \text{ X} \left(\frac{\text{Total Good Device}}{\text{Total Incoming Device}} \text{ X } 100 \right) \quad (10)$$

Equation 10 was developed to calculate the production throughput. The acquired throughput is the tested good product by considering the testing yield, which denotes the percentage of tested good products. The testing yield percentage is calculated by using Equation 7.

Equation 10 was integrated with multi-site efficiency (MSE) to compare the multi-sites and the MSE. However, this assumption was not analyzed in the paper and will be included in the next research.

To integrate the MSE into the equation, the throughput equation from Evans (1999), as shown in Equation 11, must be further enhanced. The steps to integrate the MSE into the throughput equation are discussed below.

$$UPH_{insertions} = \frac{3600 \text{ x } n}{t_{ms} + i_{ms}} \quad (11)$$

where
- t_{ms} is the multi-site test time, which is the time spent to complete testing of a semiconductor chip;
- i_{ms} is the multi-site indexing time, which is the semiconductor chip exchange time within the tested chip replaced with a new, untested chip;
- *n* is the number of test sites, which is the number of semiconductor chips tested in a single contact.

The throughput equation developed by Evans (1999) was enhanced by integrating the MSE model developed by Kelly (2008). The MSE proposed by Kelly is presented as follows:

$$MSE = \left(1\text{-} \frac{\Delta t}{\Delta N(t_1)} \right) .100\% \quad (12)$$

where
- Δt is the change in testing time between single-site and multi-site testing;
- ΔN is the number of different test sites between single-site and multi-site testing.

Equation 12 is further derived, as shown in Equation 13.

$$MSE = \left(1\text{-} \frac{(t_{MS} - t_1)}{(N\text{-}1)(t_1)} \right) .100\% \quad (13)$$

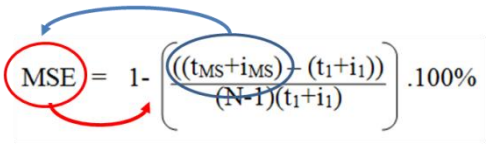
where
- t_{ms} is the multi-site test time, and t_1 is the single-site test time;
- *N* is the number of test sites for multi-site testing.

The test handler affects the testing throughput. Therefore, the test handler indexing time must be included as part of the MSE equation. Accordingly, Equation 14 was derived by including the indexing time (i) as follows:

$$MSE = 1\text{-} \left(\frac{((t_{MS}+i_{MS}) - (t_1+i_1))}{(N\text{-}1)(t_1+i_1)} \right) .100\% \quad (14)$$

To ensure effective integration of the equations, prior understanding of the relationship between the throughputs and MSE is necessary. The variables of MSE, which are related to the throughput, must be understood to determine the relationship between MSE and multi-site. Equations 11 and 14 show that the multi-site test time (t_{ms}) and multi-site indexing time (i_{ms}) are common variables in both equations.

In Equation 14, t_{ms} and i_{ms} represent multi-site test time and indexing time, respectively. Therefore, the integration process shown in Figure 3 was performed to clearly derive the relationship between t_{ms} and i_{ms} in relation to MSE.



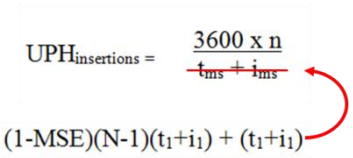
Source: Author's own research

Fig. 3 Process of deriving the relationship between t_{ms} and i_{ms} in relation to MSE.

Figure 3 illustrates that t_{ms} and i_{ms} move to the left side of the equation, whereas MSE moves to the right. The final computation for the relationship of t_{ms} and i_{ms} in relation to MSE is derived and shown in Equation 15.

$$(t_{MS} + i_{MS}) = (1\text{-MSE})(N\text{-}1)(t_1+i_1) + (t_1+i_1). \qquad (15)$$

Equation 15 was then integrated into Equation 11 to obtain the computation for testing throughput, including MSE as part of the calculation. Figure 4 depicts the computation of the integration; the complete integration is illustrated in Equation 16.



Source: Author's own research

Fig. 4 Process of computing the integration of Equation 15 into Equation 11.

$$UPH_{insertions} = \frac{3600 \text{ X } N}{((1\text{-MSE})(N\text{-}1)(t_1+i_1) + (t_1+i_1)),} \qquad (16)$$

where

$UPH_{insertions}$ are represented by the testing output in one hour.

C. Equipment Utilization (U)

Equipment utilization percentage refers to the percentage by which the test equipment is used in producing output. No cost is lost when the test equipment is 100% utilized. The aforementioned cost refers to the total cost, as indicated in Equation 9. The cost becomes cheaper when equipment utilization achieves a higher percentage. On the other hand, however, the cost increases when utilization percentage begins to decrease (Horgan, 2004).

The equipment utilization percentage affects the total cost. Thus, the former must be included in Equation 9. The total cost equation, which involves equipment utilization percentage, is depicted in Equation 17.

$$\text{Total Cost per month} = \frac{(\text{Dep} + \text{DL} + \text{OH} + C_{Pkg})}{\text{U}} \qquad (17)$$

The total cost obtained from Equation 17 is the monthly testing expenditure. However, the testing throughput is calculated based on the hourly production output. Therefore, Equation 17 must be further derived, as shown in Equation 18, to obtain the total cost per hour.

$$\text{Total Cost per hour} = \frac{\left(\frac{\text{Dep} + \text{DL} + \text{OH} + C_{Pkg}}{729.6}\right)}{\text{U}} \qquad (18)$$

where the total cost is divided by 729.6 to obtain the hourly cost, and 729.6 is the total number of production hours in one month.

All the equations and variables for average cost theory are defined. Subsequently, all equations are integrated into average cost theory to derive the cost of the model. Figure 5 illustrates the integration.

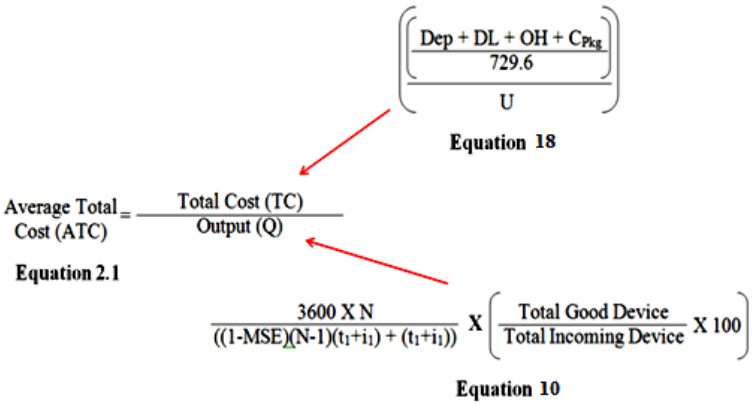


Fig. 5 Process of integrating Equations 18 and 10 into Equation 1.

Figure 5 shows that the average cost in Equation 1 is integrated with Equation 18, which is the total cost in one hour, and Equation 10, which is the total number of good chips tested in one hour.

The final cost of test model is then integrated, as shown in Equation 19.

$$CPU_{GOOD} = \frac{\left(\frac{\left(\frac{Dep + DL + OH + CPkg}{729.6}\right)}{U}\right)}{\left(\frac{3600 \times N}{((1-MSE)(N-1)(t_1+i_1)) + (t_1+i_1))}\right) \times \left(\frac{Total\ Good\ Device}{Total\ Incoming\ Device} \times 100\right)} \quad (19)$$

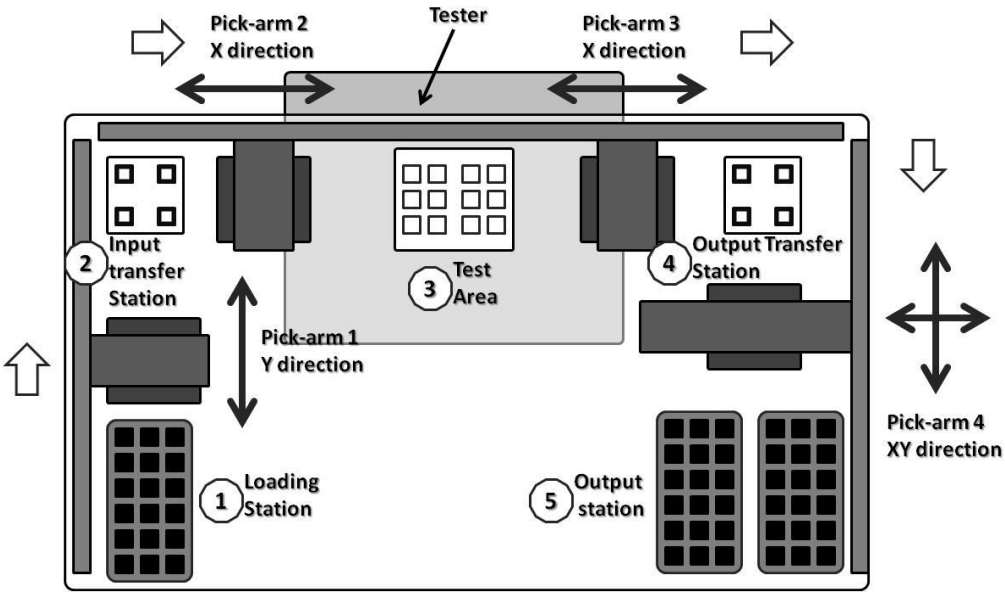
The pick-and-place test equipment and the multi-site configuration for this study are discussed in the next section.

III. PICK-AND-PLACE TEST EQUIPMENT AND MULTI-SITE CONFIGURATION

The Pick-and-place testing handling is one of the widely used methods of testing multi-sites. In this process, the semiconductor chip is already singulated from the lead frame to become an individual chip. The chip is placed on a Jedec tray to be carried from the assembly equipment to the test equipment. Figure 6 shows a photograph of Jedec trays.

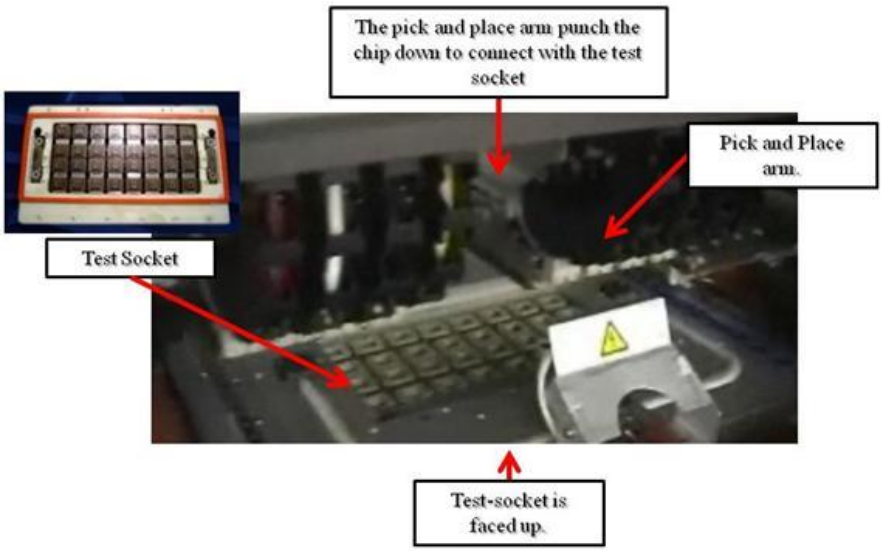
Source: Author's own research
Fig. 6 Sample Jedec trays.

The Jedec tray is loaded with semiconductor chips and then placed into the pick-and-place handler in Area 1, as shown in Figure 7.



Source: Author's own research
Fig. 7 Process flow of pick-and-place testing handling.

Pick-arm 1 transfers the chips from the tray to the input transfer station. From the input transfer station, pick-arm 2 moves the chips to the test area for testing. The pick-and-place testing handling method is different from the two previous methods, in which the tester is at the bottom and the test socket/contactor is facing up. Moreover, pick-arm 2 punches the device down instead of up to connect it with the test socket/contactor. The tested chips are then placed on the output transfer station by pick-arm 3. Finally, pick-arm 4 removes the tested chips from the output transfer station and sends them to the output station. The good and bad chips are sorted according to the test results. Figure 8 displays the test area for pick-and-place testing handling.



Source: Author's own research
Fig. 8 Test area for pick-and-place testing handling.

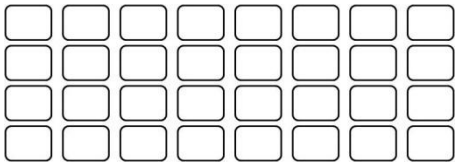
The test site configuration setup for the case study is explained in the subsequent section.

The pick-and-place test equipment can be configured from single-site to X32-sites. The test sites are configured to obtain data for the case study from single-site to X32-sites. Figure 9 displays a photograph of the pick-and-place test equipment test sites that can support X32-sites.

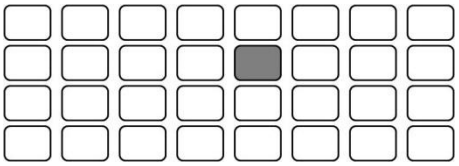
Source: Author's own research
Fig. 9 Pick-and-place test sites.

The standard layout of the test site for the pick-and-place test equipment is configured in four columns and eight rows to obtain X32-sites. With such flexibility, the test site can be configured to single-site, quad-sites, octal-sites, X16-sites, and X32-sites. The details of the configurations are described below.

From the standard test site configuration (Figure 10), the experiment first configures the test handler to pick up only one chip and to perform single-site testing to simulate the indexing and test times of the conventional testing method. Figure 11 depicts the single-site configuration (gray color indicates the test site used for testing).

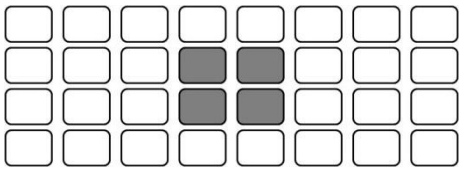


Source: Author's own research
Fig. 10 Standard layout of X32-sites.

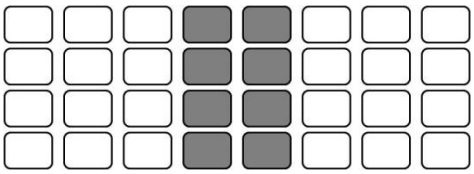


Source: Author's own research
Fig. 11 Layout of single-site.

Figures 12 and 13 show the configuration of quad-sites and octal-sites, respectively.

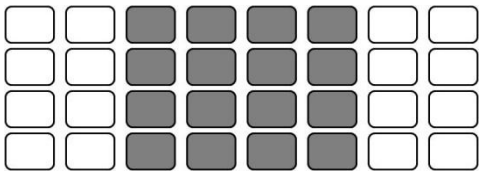


Source: Author's own research
Fig. 12 Layout of quad-sites.



Source: Author's own research
Fig. 13 Layout of octal-sites.

The test handler is configured to X16-sites (Figure 14) and X32-sites (Figure 15) when the quad-site and octal-site tests are completed.



Source: Author's own research
Fig. 14 Layout of X16-sites.

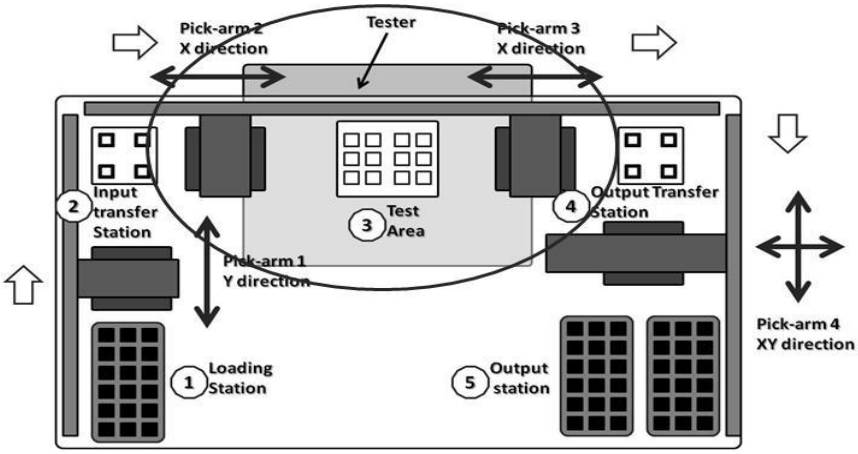
Source: Author's own research
Fig. 15 Layout of X32-sites.

The configurations of test sites are defined. The results of the analysis are discussed in the section that follows.

IV. ANALYSIS RESULT

This study considers pure indexing time only and rejects any indexing time slowed down by external factors, including the carrier transfer process, loading and unloading process, equipment jamming, and delay caused by slowing of pick-arm 1. Production data are only accepted if no external factor, including handler and tester downtimes, is identified.

This study focuses on only the area shown within the circle in Figure 16.



Source: Author's own research
Fig. 16 Focus area of this research.

The indexing time is considered valid if no waiting time exists between the exchange times for the device being tested as it is replaced with a new device before testing. However, the indexing time is considered invalid given external factors that cause immediate replacement of a new chip after the device is completely tested.

The test time is considered valid if no external factors, including tester downtime and chip contacting problems, cause a high rejection rate of the tested chip.

The data size of the 30 sets of production lots for each test site configuration (single-site, quad-sites, octal-sites, X16-sites, and X32-sites) must be collected to gather sufficient data for the cost-of-test study. Each data set contains 100 trial runs of the test equipment setup. Thus, the 30 data sets contain 3,000 test equipment trial runs. Five test site configurations are employed in both case studies. Therefore, 30 sets are used for each test site setup. The five test site configurations contain 150 data sets, including 15,000 trial runs on test equipment.

The fixed costs for this case study are tabulated in Table 1.

TABLE 1: FIXED COSTS

Variables	Cost (RM)
Depreciation cost/month	49500
Direct labor cost/month	7843
Overhead cost/month	181999

The cost of bad parts is calculated by using Equation 8, which involves an ASP of RM4.95 for the logic device. The cost of bad parts is affected by the testing yield. Table 2 depicts the summary of the cost of bad parts.

TABLE 2: COST OF BAD PARTS

Test site configurations	Cost of bad parts (RM)
Single-site	63.61
Quad-sites	110.29
Octal-sites	141.61
X16-sites	192.55
X32-sites	163.45

The results of testing throughput for pick-and-place test equipment are summarized in Table 3.

TABLE 3: TESTING THROUGHPUT FOR PICK-AND-PLACE TEST EQUIPMENT

Test site configurations	Throughput
Single-site	2659
Quad-sites	4126
Octal-sites	4447
X16-sites	4576
X32-sites	3825

Testing yield is one of the factors that affect testing cost. Table 4 shows the testing yield percentage data collected from the pick-and-place test equipment setup.

TABLE 4: AVERAGE TESTING YIELD PERCENTAGE

Test site configurations	Average Testing Yield (%)
Single-site	99.52
Quad-sites	99.46
Octal-sites	99.36
X16-sites	99.15
X32-sites	99.14

After all the required variables are obtained, the cost of good units is calculated by using Equation 19. The summary is tabulated in Table 5.

TABLE 5: COST OF GOOD UNIT.

Test site configurations	Cost of Good Unit (RM)
Single-site	0.0670
Quad-sites	0.0436
Octal-sites	0.0410
X16-sites	0.0409
X32-sites	0.0488

Data analysis by using one-way ANOVA and post-hoc test is detailed in the subsequent section.

An alpha level of 0.05 is used for the analysis. As previously discussed, five independent levels of configurations (a), namely, single-site, quad-sites, octal-sites, X16-sites, and X32-sites, are selected. Each independent level contains 30 data sets (n). In this event, the following data are determined:

a = 5 independent levels
n = 30 sets of data
N = 150

Therefore, the degrees of freedom are calculated as follows:

df between= 5 – 1 = 4
df within = 150 – 5 = 145
df total = 150 – 1 = 149

The degrees of freedom between and within that equates to (4,145), as shown in the F-Table, obtained a critical value of 2.3719. As indicated in the previous chapter, the null hypothesis is accepted if the F-value is smaller than the critical value; otherwise, the null hypothesis is rejected.

Table 5 presents the summary of the cost of good unit for pick-and-place test equipment for all test site configurations. An analysis of the hypothesis is provided in the subsequent sections.

The hypothesis for the cost-of-good-unit analysis is as follows:

H0: Improvement of the test site affects the cost of good units.
H1: Improvement of the test site does not affect the cost of good units.

The dependence level for cost of good unit is rated from a scale of 1 to 10, as shown in Table 6.

TABLE 6: SCALE OF COST OF GOOD UNIT DEPENDENCE LEVEL

Cost of Good Unit	Scale
0.0683	10
0.0655	
0.0654	9
0.0626	
0.0625	8
0.0598	
0.0597	7
0.0569	
0.0568	6
0.0541	
0.0540	5
0.0512	
0.0511	4
0.0484	
0.0483	3
0.0455	
0.0454	2
0.0427	
0.0426	1
0.0398	

The dependence level for the testing cost is on a scale from level one, which represents the cheapest cost of good unit at RM0.0398 per chip, to level ten, which represents the highest cost of good unit at RM0.0683 per chip, with a level increment resolution of RM0.0028, as shown in Table 6.

TABLE 7: ANOVA Results for Cost of Good Unit ANOVA Table

	SS	df	MS	F
Between	1667.56	4	416.89	11194.27
Within	5.4	145	0.04	
Total	1672.96	149	11.23	

Table 7 shows that the F-value is 11194.27, which is greater than the critical value of 2.3719. In this analysis, the null hypothesis is rejected. The ANOVA shows that the improvement of the number of test sites affects the cost of good unit. Thus, the cost of good units data are further analyzed by using the post-hoc test to determine the behavior of cost of good units for the entire test site setup.

TABLE 8: POST-HOC TEST ANALYSIS RESULTS FOR COST OF GOOD UNIT
Post Hoc Test

Independence Level	F-value	Analysis Result
Single vs. Quad	6284.340	Different - Reject the null hypothesis
Single vs. Octal	7916.373	Different - Reject the null hypothesis
Single vs. X16	7916.373	Different - Reject the null hypothesis
Single vs. x32	3505.174	Different - Reject the null hypothesis
Quad vs. Octal	94.093	Different - Reject the null hypothesis
Quad vs. X16	94.093	Different - Reject the null hypothesis
Quad vs. X32	402.778	Different - Reject the null hypothesis
Octal vs. X16	0.000	No Difference - Accept the null hypothesis
Octal vs. X32	886.223	Different - Reject the null hypothesis
X16 vs. X32	886.223	Different - Reject the null hypothesis

The results of the post-hoc test analysis, which are presented in Table 8, shows that the X16-sites and the octal-sites provide the cheapest cost of good unit, followed by the quad-site setup. The X32-site setup is the most expensive setup and does not provide the expected reduction in testing cost. The entire test site setup has a significant difference in the post-hoc test analysis. Thus, the null hypothesis is rejected except for the comparison between the octal-sites and the X16-sites that incurred a measurement lower than the critical value, thus fulfilling the null hypothesis condition.

V. CONCLUSION

The total cost and production output affect testing cost, as validated by this study. Production output is affected by MSE, and a higher MSE results in better production output.

The MSE is determined based on the indexing time, test time, and number of test sites. Production output increases when the indexing and test times are decreased, and the increment in the number of test sites contributes to the improvement of the production output. However, if the increment in the number of test sites affects the indexing time and test time is increased at the same time, then the MSE decreases. A lower MSE results in lower production output. Therefore, combining the three variables, namely, indexing time, test time, and number of test sites, determines the MSE, which directly contributes to the production output.

The validation process proves that increments in the number of test sites do not necessarily reduce the testing cost. This study shows that increasing the number of test sites does not guarantee improved throughput and testing cost. The main reasons for this situation are presented in Figure 17.

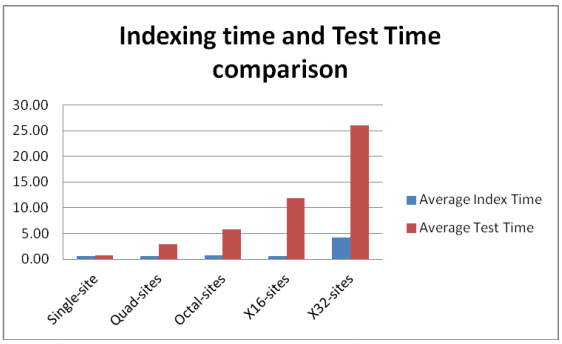


Fig. 17 Comparison of the indexing time and test time for the pick-and-place test equipment.

Testing throughput, which is the main contributor to the testing cost, is affected by the indexing and test times. Figure 17 depicts that the test time for the test equipment significantly increases once it reaches a higher test site configuration although the indexing time for the test equipment setup increases steadily. Therefore, the test time induces decreases in testing speed and testing throughput, which increases testing cost and decreases profit margin.

This study concludes that simply increasing the number of test sites is insufficient to improve testing throughput. Instead, the test time must also be reduced. The test time can be reduced through different means, including reduced pin-count testing and concurrent testing.

VI. FUTURE WORK

This study draws several future research directions that can contribute to the development of low-cost testing. The directions are briefly presented below.

A multi-site case study combined with testing time improvement methods, including concurrent testing and reducing pin-count testing, can be conducted to study the effectiveness of the combination and its contribution to the reduction of testing costs. Future research can involve collecting further data and constructing a multi-site table that can provide information on how many testing times are allowed for a test site configuration setup to reduce testing costs.

ACKNOWLEDGEMENTS

The author thanks Asia e University for the opportunity to conduct this research.

ABOUT THE AUTHOR

Khoo Voon Ching holds two master's degrees, namely, the M.Sc by research from Asia e University and a Master of Business Administration degree from Akamai University, USA. Voon Ching obtained his professional qualifications as an incorporated engineer from the Engineering Council, UK, and as a certified planning engineer from the American Academy of Project Management, USA. He also studied in the University Technology of Malaysia to obtain his diploma in Mechanical Engineering and in Institute First Robotics Industrial Science to acquire an advanced diploma in Robotics and Automation Engineering. Voon Ching is currently in pursuit of his PhD degree.

Voon Ching has many years of industry experience, specializing in automation and semiconductor testing. He first worked for ASM Assembly Equipment as a service engineer before he moved to Semiconductor Testing Automation. As a sales manager with COHU, Inc., he was involved in multi-site test handler sales and service activities. He implemented multi-site testing handlers in many MNCs involved in semiconductor testing, which primarily aimed to reduce testing costs. His research interests include technology management, cost reduction through technology, and the efficiency of technology to improve human condition.

Mr. Khoo is a member of the Institution of Mechanical Engineers and the International Associations of Engineers. He is a fellow of the American Academy of Project Management.

REFERENCES

[1] Goodall, I R.,Fandel, D., Allan, A., Landler, P., and Huff, H.R. (2002) "Long-term Productivity Mechanisms of the Semiconductor Industry," Semiconductor Silicon 2002 Proceeding of American Electrochemical society, pp. 125 – 144.
[2] Bao, G. (2003) "Challenges in Low Cost Test Approach for ARM9 Core Based Mixed-Signal SoC Dragon ball," Proceedings International Test Conference, pp. 512-519.
[3] *The Malaysian Government Valuation and Property Service Department Report 2011,* Pusat Maklumat Harta Tanah Negara (NAPIC), Putrajaya, 2011.
[4] Rivoir, J. (2003) "Lowering Cost of Test: Parallel Test or Low-cost ATE?" Proceedings of the 12th Asian Test Symposium.
[5] Evans, A.C. (1999) "Applications of Semiconductor Test Economics, and Multisite Testing to Lower Cost of Test," Proceedings of the International Test Conference, pp. 113-123.
[6] Kelly, J. (2008) "Multi-site Efficiency and Throughput," Technical Paper for Verigy.
[7] Horgan, J. (2004) "Test & ATE – Cost of Test," retrieved Nov 20, 2011, from www.edacafe.com/magazine/magazine_20040315.html.
[8] Fogiel, M, *Microeconomics*. New Jersey: Research and Education Association, 2003.
[9] Babcock, D.L, *Managing Engineering and Technology*. New Jersey: Prentice-Hall, Inc, 1996.
[10] Bruton, G.D, *The Management of Technology and Innovation.* OH: Thomson Higher Education, 2007.
[11] Lee, D.R. and Mckenzie, R.B, *Microeconomics for MBAs.* New York: Cambridge University Press, 2006.
[12] Noori, H, *Managing the Dynamics of New Technology.* New Jersey: Prentice-Hall, Inc. 1990.
[13] Turley, J, *The Essential Guide to Semiconductors.* New Jersey: Pearson Education, Inc. 2009.
[14] Thamhain, H.J, *Management of Technology.* New Jersey: John Wiley & Sons, Inc. 2005.
[15] Samuelso, P.A. and Nordhaus, W.D, *Economics.* Singapore: McGraw-Hill Higher Education, 2002.
[16] Rivoir, J. (2004) "Parallel Test Reduces Cost of Test More Effectively Than Just a Cheap Tester," Conference publication of Electronics manufacturing technology symposium, 2004. IEEE/CPMT/SEMI 29th International, pp. 263-272.
[17] Moore, G.E. (1965) "Cramming More Components onto Integrated Circuits," Proceedings of IEEE, pp. 82-85.
[18] Aizcorbe, M.A. (2002) Price Measures for Semiconductor Devices, U.S. Bureau of Economic Analysis (BEA) 2002 Working Paper Series.